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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,222	02/11/2004	Hirofumi Komori	1259-0243P	9988

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
06/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/775,222	KOMORI, HIROFUMI	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-8,10-12 and 16-20* is/are pending in the application.

4a) Of the above claim(s) *10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-7 and 16-20* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The addition of claim 20 and the cancellation of claims 15 and 16 in the amendment dated 2/7/2007 are acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of 35 U.S.C. 102(b) which forms the basis for all obviousness rejections set forth in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5 and 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent # 5625210).

Regarding claim 1, Fig. 2 of Lee et al. discloses a solid-state imaging device equipped with plural unit pixels (Col. 2, Lines 1-32) each of which includes a photo-diode 12 and a photo-detector (all features to the right of the aforementioned photodiode in Fig. 2) on a substrate 2, the photo-diode comprising a charge generating region 32 to generate charges upon light irradiation (Col. 2, Lines 23-30), the photo-detector comprising a charge accumulation region (Right half of rightmost N+ region in Fig. 2) to accumulate the charges transferred from the charge generating region 32 and a charge transfer region (channel (region beneath the gate) of RESET transistor having gate 24) provided between the charge generating region 32 and the charge accumulation region (Right half of rightmost N+ region in Fig. 2) of the pixel, and a first charge eliminating region 4 formed between the substrate 2 and the charge accumulation region (Right half of rightmost N+ region in Fig. 2), and a second charge

eliminating region 22 formed near the charge generating region, wherein the second charge eliminating region is a p+ type impurity diffusion region 22 formed on an upper surface of an n+ type impurity region 32 in the photodiode 12.

The claims to the generation of a signal potential that changes in accordance with the amount of the charges in the charge accumulation region, claims to the charge transfer region forming a first potential barrier to the charges in the charge generating region and the first potential barrier being removable according to an applied voltage to the photo-detector, claims to the first charge eliminating region forming a second potential barrier to the charges in the charge accumulation region, claims to the second potential barrier being removable according to an applied voltage to the first charge eliminating region, claims to the charges accumulated in the charge generating region being eliminated to the substrate through the charge accumulation region before starting accumulation of the charges in the charge generating region when the first and second potential barrier are removed, the claims to the charges beginning to be generated by light irradiation to the charge generating region to accumulate charges in the charge accumulation region upon formation of at least the second potential barrier, claims to the formation of the first potential barrier after a predetermined amount of time of the light irradiation preventing charges that are generated by the light irradiation to the charge generating region from being transferred to the charge accumulation region, and claims to the signal potential that changes in accordance with the amount of the charges in the charge accumulation region to be generated as a image signal are purely functional limitations. It is well known that similar structures have similar characteristics

and functions. Thus, as the device of Lee et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claims 3 and 20, Fig. 2 of Lee et al. discloses the solid-state imaging device according to claim 1, further comprising:

a region 14, provided between the charge generating region 32 and an overflow drain region 36.

The claims to the region forming a third potential barrier to the charges in the charge generating region and the third potential barrier being lower than the first potential barrier such that the charges that are overflowed from the charge generating region are eliminated via the second charge eliminating region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Lee et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 5, Fig. 2 of Lee et al. discloses the solid-state imaging device according to claim 1, wherein the charge generating region 32 has one conductive type (N), and the photo-diode 12 comprises a first region 22 with opposite conductive type (P) that contacts the charge generating region 32, and wherein the photo-detector (all features to the right of the aforementioned photodiode in Fig. 2) is a field effect transistor (see Fig. 2) and comprises:

a channel region (channel (region beneath the gate) of RESET transistor having gate 24) formed on the surfaces of the charge accumulation region (Right half of rightmost N+ region in Fig. 2) with one conductive type (p) and the charge transfer region (14) with opposite conductive type (n);

a gate electrode 24 formed on a gate insulation layer (not labeled, but seen in Fig. 2) that is formed on the channel region (channel (region beneath the gate) of RESET transistor having gate 24);

a source region 36 having opposite conductive type (n), the source region 36 near the charge accumulation region (Right half of rightmost N+ region in Fig. 2) being connected to the channel region (see Fig. 2); and

a drain region (Left half of rightmost N+ region in Fig. 2) with opposite conductive type (n) that is apart from the source region 36 by the channel region (see Fig. 2).

The claim to the signal potential being generated in the source region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Lee et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

The Examiner takes official notice that it is known in the art to form a substrate from either n-type or p-type material and then form a well of opposite type in said substrate in order to be able to form components in the desired type (n-type or p-type) of semiconductor.

Regarding claims 16-19, Fig. 2 of Lee et al. discloses the solid-state imaging device according to claims 1 and 3.

The claims to the first potential barrier being formed while at least the second potential barrier is formed and charges start to be generated by light irradiation to the charge generating region, and the first potential barrier being removed while the charges are accumulated in the charge accumulation region, and the first potential barrier being removed and formed plural times while at least the second potential barrier is formed and the charges beginning to be generated by the light irradiation to the charge generating region, to accumulate charges in the charge accumulation region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Lee et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Miida (U.S. Patent 6476371).

Regarding claims 6 and 7, Fig. 2 of Lee et al. discloses the solid-state imaging device according to claim 5, wherein the plural pixels are arranged in first and second directions to form a matrix (Col. 2, Lines 20-30) and further comprising:

Lee et al., however, fails to disclose the switch circuit capable of electrically connecting and disconnecting the source region and the drain region of the pixel and the source regions of the pixels along the first direction being connected to one another, the gate electrodes of the pixel along the second direction being connected to one another and the drain regions of all pixels being common.

Miida teaches a similar semiconductor device wherein there is a switch circuit capable of electrically connecting and disconnecting the source region and the drain region of the pixel (Miida, Col. 8, Lines 22-27 and 46-49); and

the source regions of the pixels along the first direction are connected to one another (Miida, Col. 8, Lines 2-5), the gate electrodes of the pixel along the second direction are connected to one another (Miida, Col. 7, lines 58-60) and the drain regions of all pixels are common (Miida, Col. 7, Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the switch circuit and configuration of Miida into the device of Lee et al. The ordinary artisan would have been motivated to modify Lee et al. in the above manner for the purpose of reading out a video signal that does not contain a noise component due to the remaining charges from a signal output circuit (Miida, Col. 8, Lines 8-14).

The claims to the charges in the charge accumulation region being eliminated to the substrate via the first charge eliminating region when the potentials of the charge accumulation region and the charge transfer region are increased by boosting up a voltage to the gate electrode and wherein the voltage to the gate electrode is boosted by applying a voltage to the source and drain regions simultaneously while keeping the gate electrode at a high impedance state are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Lee et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Allowable Subject Matter

4. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The closest prior art (Kawajiri et al. and Lee et al.) do not teach a second region having opposite conductive type provided between the charge generating region and the second charge eliminating region in combination with the additionally claimed features, as is claimed by the Applicant. Thus, the Applicant's claims are determined to be novel and non-obvious.

Response to Arguments

5. The substitute specification has been reviewed by the Examiner and will be entered.

Applicant's arguments regarding 35 U.S.C. 112 rejections are irrelevant as this rejection was previously withdrawn in the Office Action dated 11/15/2006.

Applicant's other arguments filed 2/7/2007 have been fully considered but are moot in view of the new grounds of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art discloses similar semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK
05/22/2007

JEROME JACKSON
PRIMARY EXAMINER